WHAT IS CLAIMED IS:

1. A method of enhancing jitter tolerance in a communications network, comprising:

providing at least two non-linear paths, a first of said non-linear paths to adjust a phase of input data in response to a data pattern of said input data, and a second of said non-linear paths to adjust said phase of said input data in response to an amplitude of data samples from said input data, and a phase locked loop to lock a phase of a local clock to said phase of said input data;

inputting data to said communications network;

estimating phase error based on said data samples from both a center of a data eye of said input data and from a phase sample from said input data half-a-baud later in time;

correlating said phase error with a sign of recovered data;

filtering said correlated phase error by a loop filter to generate an output;

summing said output with output from said non-linear paths to generate a summed output; and

converting said summed output into clock phase information.

2. The method of claim 1, further including varying a gain and bandwidth of said phase locked loop according to density of said input data and an incoming jitter frequency.

3. The method of claim 1, further including multiplying said correlated phase error by a gain prior to filtering said correlated phase error by said loop filter.

4. The method of claim 1, wherein providing at least two non-linear paths further includes providing three non-linear paths, a third of said three non-linear paths to reduce an accumulated phase error.

5. A timing recovery system to receive input data having a phase, comprising:

a phase locked loop to lock a phase of a local clock to the phase of said input data, said phase locked loop receiving said input data and generating a phase locked loop output;

a first proportional path with non-linear control to adjust the phase of said input data in response to a data pattern of said input data, said first proportional path receiving said input data and generating a first proportional path output;

a second proportional path with non-linear control to adjust the phase of said input data in response to an amplitude of data samples from said input data, said second proportional path receiving said input data and generating a second proportional path output; and

a system summing node, wherein said phase locked loop output, said first proportional path output, and said second proportional path output are summed by said system summing node to generate a system summing node output.

6. The timing recovery system of claim 5, wherein said data pattern of said input data that causes said first proportional path to adjust said phase of said input data is a string of zeros followed by a value of one in said input data.

7. The timing recovery system of claim 5, wherein said phase locked loop further includes:

a phase detector to determine said phase of said input data, said phase detector receiving said input data and generating a phase detector output; and

a loop filter to provide an additional frequency characteristic to said phase detector output, said loop filter receiving said phase detector output and generating said phase locked loop output.

8. The timing recovery system of claim 7, wherein said loop filter includes:

an accumulator to indicate a direction in which the phase error is changing, said accumulator receiving said phase detector output and generating an accumulator output; and

a loop filter summing node, wherein said phase detector output and said accumulator output are summed by said loop filter summing node, generating said phase locked loop output.

9. The timing recovery system of claim 5, wherein said timing recovery system further includes:

a third proportional path with non-linear control to reduce an accumulated phase error, said third proportional path receiving said input data and generating a third proportional path output, wherein said third proportional path output is summed by said system summing node.

10. The timing recovery system of claim 5, wherein said timing recovery system further includes an oscillator, said oscillator receiving said system summing node output and generating a final system output.

11. The timing recovery system of claim 10, wherein said oscillator is a digitally controlled oscillator (DCO).

12. The timing recovery system of claim 10, wherein said oscillator is a voltage controlled oscillator (VCO).

13. The timing recovery system of claim 10, wherein said oscillator is a digital-to-analog converter (DAC).

14. The timing recovery system of claim 8, wherein said timing recovery system further includes:

a data density detector to monitor a density of said input data, said data density detector receiving said input data and generating a data density detector output; and

a frequency detector to determine a frequency of an incoming timing jitter of said input data, said frequency detector receiving said phase detector output and generating a frequency detector output.

15. The timing recovery system of claim 14, wherein said loop filter further includes:

a phase detector gain element, said phase detector gain element receiving said phase detector output prior to said phase detector output being input to said loop filter summing node, and generating a phase detector gain element output; and

a linear gain element, said linear gain element receiving said phase detector gain element output and generating a linear gain element output, wherein said linear gain element output is input to said loop filter summing node in lieu of said phase detector output being input thereto.

16. The timing recovery system of claim 15, wherein said data density detector adjusts said phase detector gain element and said linear gain element to maintain a constant gain and bandwidth with variations in said data density, and said frequency detector adjusts a bandwidth of said phase locked loop to maximize a jitter tolerance.

17. The timing recovery system of claim 5, wherein at least one of said first proportional path and said second proportional path include at least one hold off counter.

18. A timing recovery system, comprising:

a machine-readable storage medium; and

machine-readable program code, stored on the machine-readable storage medium, the machine-readable program code having instructions to:

estimate a phase error based on a data sample from both a center of a data eye of input data and from a phase sample from said input data half-a-baud later in time;

correlate said phase error with a sign of recovered data;

filter said correlated phase error by a loop filter to generate an output;

sum said output with a path output from at least one non-linear path to generate a summed output; and

convert said summed output into clock phase information.

19. The timing recovery system of claim 18, wherein said machine-readable program code further includes instructions to vary said gain according to density of said input data and an incoming jitter frequency.

20. The timing recovery system of claim 18, wherein said machine-readable program code further includes instructions to multiply said correlated phase error by a gain prior to filtering said correlated phase error by said loop filter.

21. The timing recovery system of claim 18, wherein said machine-readable program code further includes instructions to sum said output with path output from three non-linear paths to generate a summed output.

22. A receiver system, comprising:

a receiver circuit;

an antenna in electronic communication with said receiver circuit; and

a timing recovery system circuit in electronic communication with said receiver circuit.

23. The receiver system of claim 22, said receiver system receiving input data having a phase, and said timing recovery system circuit comprising:

a phase locked loop to lock a phase of a local clock to the phase of said input data, said phase locked loop receiving said input data and generating a phase locked loop output;

a first proportional path with non-linear control to adjust the phase of said input data in response to a data pattern of said input data, said first proportional path receiving said input data and generating a first proportional path output;

a second proportional path with non-linear control to adjust the phase of said input data in response to an amplitude of data samples from said input data, said second proportional path receiving said input data and generating a second proportional path output; and

a system summing node, wherein said phase locked loop output, said first proportional path output, and said second proportional path output are summed by said system summing node to generate a system summing node output.

24. The receiver system of claim 23, wherein said data pattern of said input data that causes said first proportional path to adjust said phase of said input data is a string of zeros followed by a value of one in said input data.

25. The receiver system of claim 23, wherein said phase locked loop further includes:

a phase detector to determine said phase of said input data, said phase detector receiving said input data and generating a phase detector output; and

a loop filter to provide an additional frequency characteristic to said phase detector output, said loop filter receiving said phase detector output and generating said phase locked loop output.

26. The receiver system of claim 25, wherein said loop filter includes:

an accumulator to indicate a direction in which the phase error is changing, said accumulator receiving said phase detector output and generating an accumulator output; and

a loop filter summing node, wherein said phase detector output and said accumulator output are summed by said loop filter summing node, generating said phase locked loop output.

27. The receiver system of claim 23, wherein said timing recovery system circuit further includes:

a third proportional path with non-linear control to reduce an accumulated phase error, said third proportional path receiving said input data and generating a third proportional path output, wherein said third proportional path output is summed by said system summing node.

28. The receiver system of claim 23, wherein said timing recovery system circuit further includes an oscillator, said oscillator receiving said system summing node output and generating a final system output.

29. The receiver system of claim 26, wherein said timing recovery system circuit further includes:

a data density detector to monitor a density of said input data, said data density detector receiving said input data and generating a data density detector output; and

a frequency detector to determine a frequency of an incoming timing jitter of said input data, said frequency detector receiving said phase detector output and generating a frequency detector output.

30. The receiver system of claim 29, wherein said loop filter further includes:

a phase detector gain element, said phase detector gain element receiving said phase detector output prior to said phase detector output being input to said loop filter summing node, and generating a phase detector gain element output; and

a linear gain element, said linear gain element receiving said phase detector gain element output and generating a linear gain element output, wherein said linear gain element output is input to said loop filter summing node in lieu of said phase detector output being input thereto.

31. The receiver system of claim 30, wherein said data density detector adjusts said phase detector gain element and said linear gain element to maintain a constant gain and bandwidth with variations in said data density, and said frequency detector adjusts a bandwidth of said phase locked loop to maximize a jitter tolerance.

32. The receiver system of claim 23, wherein at least one of said first proportional path and said second proportional path include at least one hold off counter.